

Index

- Absorption laws, 20, 29
Adjacency
 column, 292
 diagram, 182
 map, 186, 293
 output, 292
 row, 292
Adjacent term, 81
Adjustable logic network, 65
Akers, S. B., Jr., 57
Algebraic determination of minimal sum, 108
Algebra of sets, 23
AND-EXCLUSIVE-OR gate combination, 55
AND gate, 42, 43
ANDNOT gate, 48
AND-NOT set, 46
Armstrong, D. B., 291, 295
Armstrong, D. B., Friedman, A. D., and Menon, P. R., 155
Ashenhurst, R. L., 68
Associative laws, 20, 47, 48
Asynchronous operation of sequential circuits, 126, 229
Bartee, T. C., 118
Bartee, T. C., Lebow, I. L., and Reed, I. S., 255
Basis, for minimization techniques, 80
Baugh, C. R., et al., 68
Bias
 input, 61
 weight, 64
Binary adder, 53
Binary addition, 6, 7
Binary arithmetic, 6–11
Binary bit, 7
Binary codes, 11–14
Binary counter, 247, 263–265
Binary division, 10, 11
Binary multiplication, 9, 10
Binary number system, 3, 4
Binary operations, 18, 19, 47
Binary sequence generator, 252–254
Binary serial adder, 232, 237, 256–258
Binary signal representation, 125, 126
Binary subtraction, 7–9
Bit time, 256
Boolean algebra, 19–23
Boolean function, 23
Booth, T. L., 255
Bowman, R. M., and McVey, E. S., 118
Branching method, 106
Burke, R. E., and Bosse, J. G., 68
Cadden, W. J., 128
Caelingeart, P., 55, 57
Caldwell, S. H., 165
Canonical EXCLUSIVE-OR and EXCLUSIVE-NOR expressions, 53
Canonical function form, 23, 32–37
Canonical product-of-sums expression, 33
Canonical sum-of-products expression, 33
Characteristic numbers, 33, 55
Chu, Y., 6, 255
Chuang, Y. H., 265
Clear input, 238
Clocked fundamental mode, 230–234
Clocked pulse mode, 234–240
Clock input, 229
Closed-cycle operation, 179
Closure property
 of binary operator, 19
 in flow table reduction, 278
Coates, C. L., and Lewis, P. M., 60
Codes
 binary, 11–14
 cyclic, 13
 distance between, 81
 Gray, 13, 14
 reflected binary, 13, 84
 self-complementing, 12
 triangle rule, 184
 unweighted, 12
 weighted, 11, 12
Coincidence, 47
Column adjacency, 292
Column dominance, 104–108, 114
Commutative operations, 19, 47, 48
Compatible row pairs, 278
Compatibles
 lower bound on the number of, 285
 splitting of, 286
 upper bound on the number of, 285
Complementary expression, 30
Complementation laws, 20
Complete cyclic code, 14
Completely specified function, 95
Consensus, 21, 93
Consensus term, 30, 31, 147, 149
Core terms, 103
Critical race, 144, 145, 181, 210, 214, 223, 230
Crowley, T. H., 295
Cyclic codes, 13
Cyclic prime implicant table, 106, 116
Davis, W. A., 296
Decimal-binary conversion, 5, 6
Decimal numbers in the Karnaugh map, 85

- Decimal symbols for the representation of functions, 33
- Delay in signal propagation, 79
hazard due to, 146–152
in pulse-mode operation, 208, 209
in sequential circuit modeling, 128, 129
- De Morgan's laws, 27
- Direct-set (reset) flip-flop input terminal, 198,
- Disjunctive terms, 35, 37, 148
- Distance between codes, 81
- Distinct code assignments, 290, 291
- Distinct codes, 288
- Distinguished cells, 92, 94, 97, 98, 112
- Distinguished columns, 102
- Distributive law, 19, 29
- Dominance relations, 104–108, 114, 115
- Don't care conditions, 96
- Double-rail device, 142
- Double-rail logic, 43
- Double-rank register, 232
- Dual gate functions, 66
- Duality principle, 20
- Duley, J. R., and Dietmeyer, D. L., 265
- Earle, J., 67
- End-around carry, 9
- Equivalence function, 47
- Equivalence-set, 275
- Equivalent states, 174–176
- Essential hazards, 152–155, 210, 223
in pulse mode operation, 210
- Essential prime implicant, 92, 93, 95, 103
- Essential row, 103
- Essential subcube, 92
 - Excess-3 code, 12, 13
 - Excitation equations, 191–199
 - Excitation functions, 140
 - Excitation table, 141–143
 - EXCLUSIVE-NOR canonical expression, 53–58
 - EXCLUSIVE-NOR circuits, 53–59
 - EXCLUSIVE-NOR gate, 48
 - EXCLUSIVE-OR canonical expression, 53–59
 - EXCLUSIVE-OR circuits, 53–59
 - EXCLUSIVE-OR gate, 48
 - Expansion theorems, 28, 31, 32, 36
 - Fan-in, 43, 48
 - Fan-out, 43
 - Feedback, 124, 127
 - Feedback loop delay, 128, 129, 132, 134, 136, 181, 214
 - Flip-flop
design for operation in pulse mode, 220–223
direct input terminals, 198
double-rank, 221
master-slave, 221
type JK, 241–248
type RS, 141–143, 192–199, 241–247, 258–261
type RST, 241–247
type T, 241–247, 263–265
 - Flow table, 134, 136
covering requirements, 274
formation for operation in fundamental mode, 165–173
formation for operation in pulse mode, 210–217
initial state, 173, 174
reduction, 173–181, 274–287
redundant rows, 174
strongly connected, 171
 - Forbidden input combinations, 96
 - Formal implication, 26, 47
 - Friedman, A. D., Graham, R. L., and Ullman, J. D., 191
 - Full adder circuit, 53, 54
 - Functional completeness, 46, 49, 53
 - Functions
number of, 68
of two variables, 46, 47
 - Fundamental mode of circuit operation, 126, 131, 143, 144, 179, 198, 223
clocked, 230–234
 - Fundamental terms, 32
 - Gain in feedback loop, 138, 139
 - Gardner, M., 3, 84
 - Gate
AND, 42, 43
ANDNOT, 48
EXCLUSIVE-NOR, 48, 53
EXCLUSIVE-OR, 48, 53
NAND, 48, 49
NOR, 48, 49
NOT, 42, 43
OR, 42, 43
ORNTO, 48
sharing, 110, 114, 115, 183
 - Generic variable, 23
 - Gimpel, J. F., 118
 - Grasselli, A., and Luccio, F., 286
 - Gray codes, 13, 14
 - Half-adder circuit, 53
 - Half-pulse hazard, 249

- Hartmanis, J., and Stearns, R. E., 296
 Hazards
 essential, 152–155, 210, 223
 static. *See* Static hazards
 Hellerman, L., 68
 Hlavíčka, H., 155
 Hopcroft, J. E., 65
 Huffman, D. A., 126, 129, 190, 191, 275,
 276
 Hyperplane, 64

 Idempotent laws, 20
 Identity elements, 19
 Implication, formal, 26, 47
 Implication table, 278
 Impossible sequential circuits, 125, 173,
 219
 Inaccessible state, 174, 176
 INCLUSIVE-OR function, 47
 Incompatible row pairs, 278
 Incompletely specified functions, 95
 Information transfers in sequential circuit
 design, 255–265
 Initializing input, 174, 238
 Internal race problem, 144, 145
 Internal state, 129
 Intersection of sets, 23
 Inversion, 42
 Inverter, 43
 Irredundant sum, 81
 Iterated consensus, 109, 110, 118

 JK flip-flop, 241–248
 Johnson, D. L., and O'Keefe, K. H., 296

 Karnaugh, M., 84
 Karnaugh map
 adjacent cells in, 84
 decimal labeling, 85
 determining multiple-output prime impli-
 cants from, 112
 determining prime implicants from, 87–92
 determining prime implicants from, 89
 distinguished cells, 92, 94, 97, 98, 112
 optional entries, 96–98
 selection of subcubes from, 92–95
 subcubes in, 87–91
 writing minimal products from, 95
 writing minimal sums from, 92–95
 Kella, J., 286

 Leading edge, of pulse, 126
 Leading-edge triggering, 220, 222
 Linearly-separable switching function,
 60, 64

 Linear-separable logic, 60
 Literal, 27, 52, 79
 Logic
 circuits, 42–46
 gain, 49
 modules, 67
 negative, 66
 positive, 66
 symbols, 43
 transition, 265
 Logical addition, 27, 42
 Logical multiplication, 27, 42
 Loomis, H. H., 46

 McCluskey, E. J., 99, 126, 165, 174
 McCulloch, W. S., and Pitts, W., 60
 Maki, G. K., and Tracey, J. H., 188
 Marihigh, G. E., and Anderson, R. E., 92
 Maximal compatibility class, 278
 Maximal compatibles, 280
 Maximal incompatibles, 285
 Maxterm, 32
 Mealy, G. H., 126
 Merger diagram, 177
 Miller, J. E., 2
 Minimal logic circuits, 67–69, 79
 Minimal sets of prime implicants, 92–95
 Minimal sets of prime implicants, 95
 Minimal sum by algebraic determination,
 108
 Minnick, R. C., 65
 Minterm, 32
 Module, logic, 67
 Moore, E. F., 68, 126
 Mott, T. H., 109
 Mukhopadhyay, A., and Schmitz, G., 58
 Multiple-output circuits, 110–118
 Murago, S., and Takasu, S., 63, 65, 66

 Nadler, M., 84
 NAND circuits, 49–52
 NAND gates, 48, 49
 Narasimhan, R., 286
n-ary operations, 47, 49
n-dimensional cube, 64, 82
 Necula, N. N., 118
 Negative logic, 66, 78
 Next-state functions, 133, 140, 141, 143
 Next-state variables, 129
 Nichols, A. J., 296
 Nickels, A. J., and Armstrong, D. B., 295
 Nodes, additional, 184, 188–190
 Noncritical race, 144
 Nonrestoring binary division, 10, 11

- NOR circuits, 49-52
- NOR gates, 48, 49
- NOT gate, 42, 43
- Null set, 23
- Number representation, 3, 4
- Number system conversion, 4-6

- Octal number system, 3, 4
- Octal representation of canonical terms, 100-102
- Odd-level gate inputs, 51, 52
- One's complement, 8, 9
- Open-loop characteristic, 138, 139
- Optimal circuit, 67
 - realization, 79
- Optional entries, 96-98, 136
- Optional terms in Quine-McCluskey technique, 101, 104
- OR gate, 42, 43
- ORNOT gate, 48
- OR-NOT set, 46
- Output adjacencies, 292
- Output assignments to avoid momentary false outputs, 167
- Output table, 130

- Parallelogram rule, 64
- Partial pulses, 249
- Paull, M. C., and Unger, S. H., 275, 278, 286
- Paull, M. C., and Waldbaum, G., 286
- Perfect induction, method of, 27, 28, 38
- Peterson, W. W., and Weldon, E. J., Jr., 13
- Petrick, S. R., 108, 116
- Petrick's method, 108, 116
- Pierce arrow function, 47
- Positive logic, 66, 78
- Postulates of Boolean algebra, 19, 20
- Present-state variables, 129
- Prime-implicant function, 108, 116
- Prime implicants
 - complete sum of, 89
 - core of, 103
 - definition of, 88
 - essential, 92, 95, 97, 103-106, 112
 - minimal sum of, 92-95
 - multiple output, 112
 - secondary essential, 103, 105, 106
 - table of, 102-108
- Prime implicants, 89
- Primitive flow table, 136, 166
 - minimum row, 176, 275
- Product-of-sums expression, 33, 37
- Propositional logic, 23, 24-27

- Pseudoequivalence, 276
- Pulse
 - leading edge, 126
 - trailing edge, 126
- Pulse-mode operation of sequential circuits, 126, 144, 210

- Quine, W. V., 99, 118
- Quine-McCluskey technique, 99-102
 - using octal symbols, 100-102

- Race conditions, 144, 145
- Radix point, 3
- Ramamoorthy, C. V., 58
- Redundant rows, 174
- Reed, I. S., 256
- Reflected binary code, 13
- Register, 255
- Resolution time, 144, 229, 249
- Richards, R. K., 6, 11
- Ricketts, A. W., Jr., 63
- Ring sum function, 47
- Row, essential, 103
- Row adjacencies, 292
- Row dominance, 104-106, 114, 115
- Row merging, 177-181
- Row sets, 190
- RS flip-flop
 - application table, 193
 - characteristics, 141
 - excitation equations, 191-199
 - gating costs, 243-247
- RST flip-flop, 241-247
- Russo, R. L., 67

- Schorr, H., 265
- Secondary essential prime implicant, 103, 105, 106
- Self-complementing codes, 12
- Sequence generator, 252-254
- Sequential circuit
 - analysis, 124-155
 - asynchronous operation, 126, 229
 - clocked, 229-240
 - closed cyclic operation of, 179
 - control states in design of, 252-255
 - memory characteristics, 124, 127
 - model, 128, 140
 - modes of operation, 126
 - physical requirements, 137, 138, 139
 - resolution time, 144, 229, 249
 - shift-register realizations of, 296
 - stable state, 129

- Sequential circuit (continued)
 state-point motion, 131, 144
 synchronous operation, 126, 229
 total state, 130
- Serial binary adder, 232, 237, 256–258
- Sets
 algebraic, 23–25
 row, 190
- Shannon, C. E., 28
- Sheffer-stroke function, 47
- Shift register, 230, 236
- Single-rail logic, 43
- Slagle, J. R., Chang, C.-L., and Lee, R. C., 118
- Sling, 145
- Smith, J. R., Jr., and Roth, C. H., 265
- Smith, R. A., 68
- Split pulse, 249
- Stabler, E. P., 265
- Stable state, 129
- Standard logic modules, 67
- State
 diagram, 145, 146
 discrete, 1
 stable, 129
 total, 130
- State assignments, 287–296
 partitioning techniques in, 295
- Static hazards
 in flip-flop circuits, 198, 199
 in gate circuits, 146–152, 214
- Subcubes, 83
 essential, 92
 selection of, 92–95
- Subsuming terms, 83, 109, 110
- Sum-module-two operation, 47
- Sum-of-products expression, 33, 37
- Switching algebra, 27
- Switching functions
 classes of, 68
 geometric representation, 82
 incompletely specified, 95–98
 number of, 68
- Synchronizing circuits, 248–252
- Synchronous operation of sequential circuits, 126, 229
- Table of combinations, 32, 33
- Tan, C.-J., 296
- Term
 adjacent, 81
 core, 103
 definition of, 23
- Theorems in n variables, 27
- Threshold adjustable-logic networks, 65
- Threshold element
 bias, 61
 circuits, 59–66
 weights, 60
- Threshold function inequalities, 61–64
- Time-difference equations, 256
- Tison, P., 109
- Tracey, J. H., 191
- Trailing edge of pulse, 126
- Trailing-edge triggering, 223
- Transfer notation, 256
- Transition
 arrow, 145
 diagram, 182
 table, 181
- Transition logic, 265
- Trigger flip-flop, 241–247, 263–265
- Two-level circuit realizations, 45, 79
- Two's complement, 8
- Unger, S. H., 154, 191, 285, 286
- Union of two sets, 23
- Universal set, 23
- Unstable state, 129
- Veitch, E. W., 85
- Venn diagrams, 24, 25
- Weighted codes, 11, 12
- Weight-threshold vector, 61
- White, S. A., 66
- Wood, O. L., 48
- Yau, S. S., and Tang., C. K., 67